# *INTEGRAL UNIVERSITY LUCKNOW*

*Department of Electronics Engineering*

Digital Electronics

## ASSIGNMENT-3(Part -B)

Course:B.Tech. Unit. 1
Branch/ Sem: _____ Session-201__-1__
Faculty-Qazi S. Ahmad Date of issue-_____
Subject Code: IEC-401/IEC-305 Date of Submission-_____

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Ques.1 Convert the following decimal no into binary no using sum of weights method
(a) 14 (b) 30 (c) 60 (d) 90

Ques.2 Convert the following decimal no into binary no.
(a) 36.1875 (b)0.625 (c) 0.1875 (d) 0.5625

Ques.3 finds the following values
$(786.983)_{10}=(x)_{16}$
$(82.35)_{10}=(x)_{4}$
$(77.43)_{10}=(x)_{6}$

Ques.4 Convert the following binary no. into decimal no. And octal no.
(a) 1101.011 (b) 11101.101 (c) 1011101.0111

Ques.5 Convert the following octal no. into decimal no.
(a) 763.45 (b) 467.342 (c) 23.734

Ques.6 Convert the following Hexadecimal no. into decimal no.
(a) ABC.75 (b) 765.ECE (c) 73.20

Ques.7 Convert the following binary no. into hexadecimal no.
10111011.1101101 And 101110111.10110110

Ques.8 Find the 10's complement of the given decimal no.
(a) 7634 (b) 76.34 (c)0.456

Ques.9 Find the 9's complement of the given decimal no.
(a) 7543 (b) 632.456 (c) 0.7863

Ques.10 Find the 1's &2's complement of the given binary no.
(a) 11011 (b) 1101.01 (c) 0.1010 (d) 10110

Ques.11 Perform the following using 10's complement
76532-4250 And 4250-76897

Ques.12 Perform the following using 2's complement and in ES-3 code.
1110-1100 And 1100-110111

# ***INTEGRAL UNIVERSITY LUCKNOW***

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Digital Electronics

ASSIGNMENT-1

Course:B.Tech. Unit. 1
Branch/ Sem: _____ Session-201_-1_
Faculty-Qazi S. Ahmad Date of issue-_____
Subject Code: IEC-401/IEC-305 Date of Submission-_____

**Ques.1** What do you mean by different wave shaping techniques? Explain different techniques of it?

**Ques.2** What do you mean by High – pass RC circuit? Show it response for the following input wave.

(a) Sinusoidal
(b) Step
(c) Pulse
(d) Square wave

**Ques.3** Derive the Transfer function for the High pass and Low pass filter circuit.

**Ques.4** How the High – pass RC circuit can be used as Differentiator?

**Ques.5** Prove that when C and R is interchanged **in** High – pass RC circuit then it will work as Low pass filter circuit.

**Ques.6** How the Low – pass filter can be used as Integrator?

**Ques.7** What do you mean by compensated attenuator? Explain.

**Ques.8** Show the response of low pass filter for the following input wave.

(a) Sinusoidal
(b) Step
(c) Pulse
(d) Square wave

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ASSIGNMENT-4

Course:B.Tech. Unit. 2
Branch/ Sem: _____ Session-201_-1__
Faculty-Qazi S. Ahmad Date of issue-_____
Subject Code: IEC-401/IEC-305 Date of Submission-_____

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**Ques.**1What do mean by logic family? Write different classes of logic family.

**Ques.**2 Design NAND and NOR gate using RTL and DTL logic family and explain its operation.

**Ques.**3 How BJT, MOSFET and Diode can be used as switch?

**Ques.**4Define the following terms
(a) Noise margin Noise immunity
(b) Fan In and Fan Out
(c) Propagation gate delay
(d) Figure of merit

**Ques.**5 Design NAND and NOR gate using DCTL logic family and explain its operation.

**Ques.**6What do you mean by wired logic? How wired AND wired OR logic can be obtained?

**Ques.**7 Design NAND and NOR gate using HTL logic family and explain its operation.

**Ques.**8What are different types of TTL series write their name only.

**Ques.**9 Design CMOS NAND, CMOS NOR gate and CMOS inverter gate.

**Ques.**10 Design TTL NAND gate and compare them using
(a) Totem pole output
(b) Open collector output
(c) Tristate output

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## ASSIGNMENT-3(Part-A)

Course:B.Tech. Unit. 3
Branch/ Sem: _____ Session-201_-1_
Faculty-Qazi S. Ahmad Date of issue-_____
Subject Code: IEC-401/IEC-305 Date of Submission-_____

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**Ques.**1Implement Half adder using NAND and NOR gate only and write their expression.

**Ques.**21Implement Full adder using NAND and NOR gate only and write their expression.

**Ques.**3 Implement Half and Full subtractor and write their expression.

**Ques.**4Draw binary 4 bit Adder/ subtractor and explain its operation.

**Ques.**5What do you mean by carry look ahead adder? Explain

**Ques.**6 Design 4 bit -BCD adder.

**Ques.**7 Implement binary to BCD and BCD to Excess-3 code converter.

**Ques.**8 Implement 2-bit and 4-bit magnitude comperator.

**Ques.**9Design a 5 to 32 decoder using one 2 to 4 and four 3 to 8 decoder ICs.

**Ques.**10 Implement the following function using:

(a) 16:1MUX
(b) 8:1MUX
(c) 4:1MUX
(d) 2:1MUX

**Ques.**11 Implement the full adder 1 to 8 demultiplexer.

**Ques.**12 Design the full adder 8 to 1 multiplexer ICs

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ASSIGNMENT-5

Course:B.Tech. Unit. 4&5
Branch/ Sem: _____ Session-201_-1_
Faculty-Qazi S. Ahmad Date of issue-_____
Subject Code: IEC-401/IEC-305 Date of Submission-_____

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**Ques.**1What is the difference between combinational logic and sequential logic circuit.

**Ques.**2What is the difference between Flip-Flop and Latch.

**Ques.**3Convert the following Flip-Flop:

(a) RS into D
(b) RS into T
(c) RS into JK
(d) JK into T
(e) JK into D

**Ques.**4 Explain different types of shift registers.

**Ques.**5Design mod-5 counter using JK Flip-Flop and implement it.

**Ques.**6Design a counter using T Flip-Flop that goes through following repeated sequence 0, 1, 3,7,6,7

**Ques.**7 Explain the different types of semiconductor memories.

**Ques.**8 Implement the following in PLA

$F_1(A,B,C)=\sum(0,1,2,4,7)$
$F_2(A,B,C)=\sum(0,5,6,9)$

**Ques.**9 Implement the following function in PAL

$F_1(w, x, y,z)=\sum(0.2.6.8.12.13)$